

000101 523350

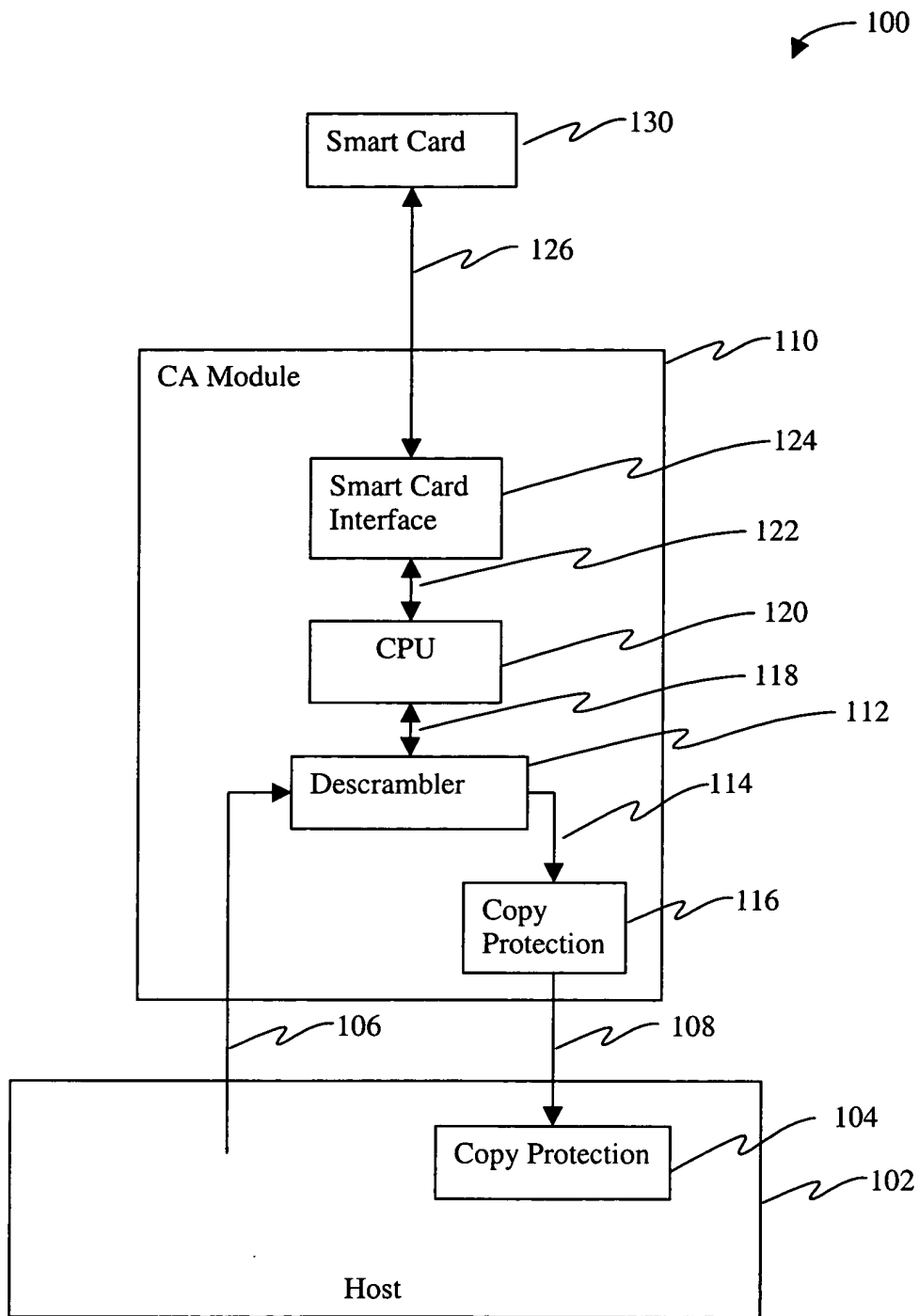


Figure 1 (Prior Art)

```

graph TD
    subgraph Host [200]
        202[Host Enclosure]
        212[Descrambler]
        220[CPU]
        224[Smart Card Interface]
        218[ ]
        222[ ]
    end
    230[Smart Card]
    226[ ]
    206[Input]
    214[Output]

    230 <--> |226| 224
    224 <--> 220
    220 <--> 212
    206 --> 212
    212 --> 214

```

Figure 2

100-443887-100

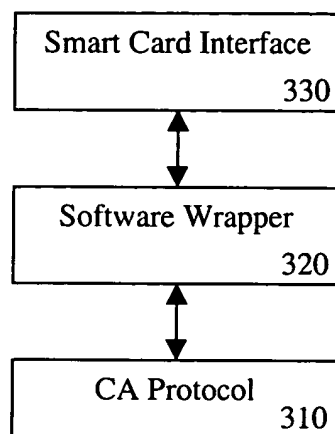


Figure 3

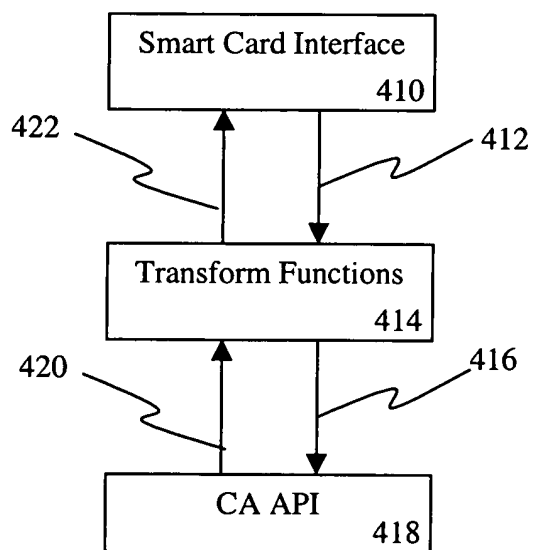


Figure 4

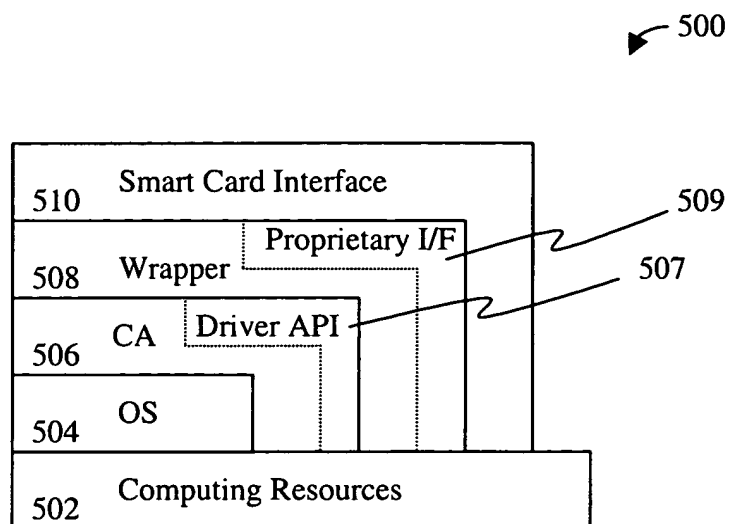


Figure 5

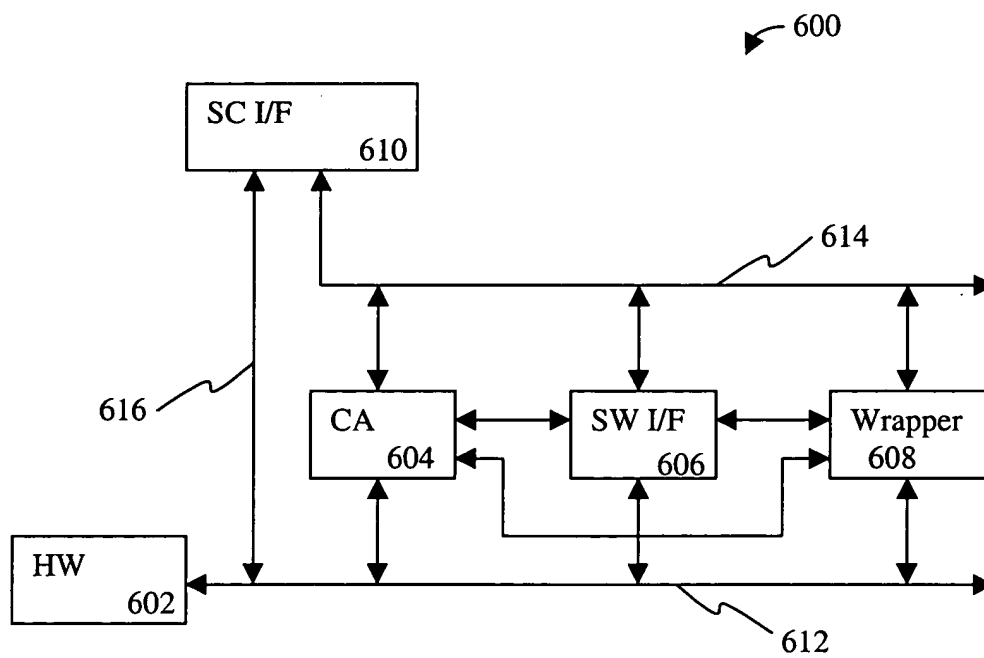


Figure 6